Amendments to the Specification:

Please replace the paragraph beginning at col. 2, line 52 with the following amended paragraph:

At this time, assume that the data SA0 through SA7 outputted from the sense amplifier is "11011100". Then, since data SA1 and SA5 which are the second bit and the sixth bit, respectively, are different from each other, the data outputted via the output terminals of the exclusive NOR gates EG1 through EG8 become "10011000". As a result, the output of the NOR gate NG is maintained at a low level, and a re-programming operation is performed. At the same time, the data "101111011" outputted via the output terminals of the exclusive NOR gates EG1 through EG8 is latched to the flip-flops F1 through F8 respectively depending on the input of the program state signal PGM4, and the output signals Q0 through Q7 of the flip-flops F1 through F8 are inputted to the NOR gates N1 through N8, respectively. For reference only, before the data "10111011" ["101111011"] is inputted to the data latch circuit 2, the flip-flops F1 through F8 are maintained at the state in which the data of "0" is latched by the input of the power-up reset signal PURST. Thereafter, the data "10011000" outputted from the flip-flops F1 through F8 are inputted to the NOR gates N1 through N8 of the control circuit for generating high voltage 3 respectively, and the output data "1001100" of the data input buffer is inputted to the inverters I1 and I8, respectively.